IN THE CLAIMS:

Kindly replace the claims of record with the following full set of claims:

1. (Currently amended) A receiver signal strength indication circuit receiving a discretely controlled amplified signal from an amplifying means (A1-A4), the circuit comprising:

~~means (A1-A4) for discretely controlled amplifying an input signal;~~

narrow filter means ~~(NF, log, ADC)~~ coupled to an output of [[the]] discretely controlled amplifying means (A1-A4), said narrow filter means providing a limited spectrum of the input signal;

logarithmic detector means for receiving and logarithmically amplifying an output of the narrow filter; and

ADC means for converting the output of the logarithmic detector to a digital ~~for furnishing a~~ receiver signal strength indication.

2. (Cancelled)

3. (Original) An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2, M) include selectivity filtering means (SF1, SF2).

4. (Currently amended) An integrated tuner comprising a receiver signal strength indication circuit as claimed in claim 1, wherein the amplifying means (A1-A4, SF1, SF2, ~~M~~) include a mixer (M).